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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,068	09/25/2003	Wilson Y. Liao	INTCP004	5861

45460   7590   05/29/2007

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EXAMINER
MOUTAOUAKIL, MOUNIR

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
05/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)
Office Action Summary		10/671,068	LIAO ET AL.
		Examiner	Art Unit	
		Mounir Moutaouakil	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 September 2003</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-20</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-20</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>25 September 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

. 1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1, 4-7, 9-11, 13, and 16-19 are rejected under 35 U.S.C. 102(b) as being

anticipated by Gaddis et al (US 5,815,501). Hereinafter referred to as Gaddis.

Regarding claim 1. Gaddis discloses an ATM-Ethernet network system (see

figure 1). The system comprises an ATM processor (see figure 3, ATM cell processor);

an Ethernet network processor (see figure 3, Ethernet controller); and an ATM-Ethernet

processor interfacing between the ATM processor and the Ethernet network processor

(see figure 1, ATM-Ethernet portal, also see figure 3, which is a schematic block

diagram of the ATM Ethernet portal hardware architecture, see the control

microprocessor). The ATM-Ethernet processor includes a packet buffer pointer ring for

managing traffic from the Ethernet network processor to the ATM processor the packet

buffer pointer ring to contain a plurality of ATM processor packet buffer pointers (See

figure 3 and column 5, lines 25-67. the system manages and controls manages frames

traffic), a packet descriptor ring and a data buffer for managing traffic from the ATM

processor to the Ethernet network processor, the packet descriptor ring being

configured to contain a plurality of packet descriptors each including an ATM-Ethernet

packet buffer memory address in the data buffer (See figure 3 and column 5, lines 25-

column 6 lines 17. packet descriptor is used to manage the cell flow from the ATM network to Ethernet network).

Regarding claim 4. Gaddis discloses a system where the packet buffer pointer ring is hardware scalable in size (see figure 3, see column 5 lines 1-24. where all of the elements implemented are hardware scalable in size).

Regarding claim 5. Gaddis discloses a system where the packet buffer pointer ring is a hardware FIFO to contain packet buffer pointers that point to packet buffer memory locations in the memory of the ATM processor (see figure 4 and see column 6, lines 1-16. the packet buffer pointer is a hardware FIFO, and points to packet buffer memory location of the ATM processor).

Regarding claims 6 and 14. Gaddis discloses a system where each packet buffer pointer contains a flag to signal to the ATM-Ethernet processor hardware whether the packet buffer pointer is being used (see column 5; lines 25-46. the DMA controller is used to flag the ATM-Ethernet microprocessor whether new cells have arrived).

Regarding claim 7. Gaddis discloses a system where each packet buffer pointer points to a packet buffer memory location in a memory of the ATM processor (see column 6 lines 1-17. the system points to a packet buffer memory location in a shared memory of the ATM processor).

Regarding claims 9 and 15. Gaddis discloses a system where the packet buffer pointer ring and the packet descriptor ring are implemented as circular FIFOs (see figure 4).

Regarding claim 10. Gaddis discloses a method for data communication. The

method for data communication comprises receiving a packet from a network processor

by an ATM-Ethernet processor for transmission to an ATM processor (see figure 3);

fetching a packet buffer pointer from a packet buffer pointer ring of the ATM-Ethernet

processor, the packet buffer pointer including a memory address pointing to a packet

buffer memory location in a data buffer memory of the ATM processor; and transmitting

the fetched packet buffer pointer and the received packet to the ATM processor (See

column 5, lines 54-67).

Regarding claim 11. The method of Gaddis further comprises identifying the

memory in the ATM processor to which the memory address in the fetched packet

buffer pointer points by the ATM processor; storing the packet to the memory identified

in the ATM processor; and returning the packet buffer pointer to the ATM-Ethernet

processor for reuse (see column 5, lines 54-67. the microprocessor manages the cells

by locating, storing and transmitting the cells to the memory locations assigned.

Moreover, pointers are received to be recycled).

Regarding claim 13. Gaddis discloses a method where the packet buffer pointer

ring of the ATM-Ethernet processor is hardware scalable in size (see figure 3, see

column 5 lines 1-24. where all of the elements implemented are hardware scalable in

size).

Regarding claim 16. Gaddis discloses a method for data communication. The

method comprises: receiving a packet from an ATM processor by an ATM-Ethernet

processor for transmission to a network processor; storing the packet in a data buffer of

the ATM-Ethernet processor; storing a packet descriptor for the packet in a packet

descriptor ring of the ATM-Ethernet processor, the packet descriptor including a pointer

to a memory location in the data buffer to which the packet is stored; analyzing the

packet descriptor for error; and if error is detected: dropping the packet descriptor;

reporting error to the ATM processor; if no error is detected: fetching the packet from

the data buffer of the ATM-Ethernet processor; and transmitting the packet to the

network processor (see column 6, lines 1-17).

Regarding claim 17. The method of Gaddis further comprises returning the

packet descriptor to the packet descriptor ring for reuse (see column 6, lines 15-17).

Regarding claim 18. Gaddis discloses a method where the packet descriptor ring

of the ATM-Ethernet processor is hardware scalable in size (see column 5, lines 14-24.

and see figure 3).

Regarding claim 19. Gaddis discloses a method where the packet descriptor ring

is implemented in the ATM-Ethernet processor as a circular FIFO (see figure 4).

Claim Rejections - 35 USC § 103

3.   This application currently names joint inventors. In considering patentability of

the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g)

prior art under 35 U.S.C. 103(a).

4.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating
obviousness or nonobviousness.

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set
forth in section 102 of this title, if the differences between the subject matter sought to be patented and
the prior art are such that the subject matter as a whole would have been obvious at the time the
invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Gaddis in view of Vogel (US 6,075,788).

Regarding claim 2. Gaddis discloses an ATM data processor, which is an ATM l2

processor.

Regarding claim 2 and 12. The system of Gaddis discloses all the limitations of

claims 1 and 10. Gaddis does not disclose that the ATM processor is in communication

with the SONET framer. However, Vogel discloses a method of communicating ATM

network and SONET network (See column 2, lines 62-67). Thus, it would have been

obvious to the person of ordinary skill in the art at the time of the invention to add a

SONET framer, as suggested by Vogel, to communicate with the ATM processor in

order to receive ATM cells and load them into synchronous payload envelopes (SPE)

forming SONET frames.

7.   Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaddis.

        Regarding claim 3. Gaddis discloses all the limitations of claim 1.

        Gaddis does not comprise an Ethernet MAC in communication with the Ethernet

network processor. However, the examiner takes official Notice that it is well known in

the art to have an Ethernet network processor in communication with an Ethernet MAC

to provide services to clients or local area networks.

8.   . Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaddis in

view Yoaz et al (US 2004/0215934). Hereinafter referred to as Yoaz.

        Gaddis discloses using descriptors as pointers to manage the conversion form

the Ethernet controller to the ATM cell processor.

        Gaddis does not disclose that the packet pointer contains 16 bits, 15 of which

being for a pointer to point to a packet buffer memory location in a memory of the ATM

processor. However Yoaz discloses a system where the packet pointer contains 16 bits

(see paragraph 18). Thus, it would have been obvious to the person of ordinary skill in

the art at the time of the invention to implement the packet pointer of Gaddis using 16

bits, of which 1 bit can be used as a flag and the rest can be used as address location,

as suggested by Yoaz. Moreover, long pointer has the advantage of greater memory

location access than a shorter length pointer.

9.   Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaddis

in view of Rozario et al (US 6,618,793). Hereinafter referred to as Rozario.

Gaddis discloses the use of packet descriptors.

Gaddis does not disclose that packet descriptor contain 8 bytes (64 bits) (see

column 4, lines 5-12). However, Rozario discloses a packet descriptor containing 8

bytes. Thus, it would have been obvious to the person of ordinary skill in the art at the

time of the invention to use 8-byte packet descriptor to indicate the location in a

memory.

Conclusion

10.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. See PTO-892.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Mounir Moutaouakil whose telephone number is 571-

270-1416. The examiner can normally be reached on Monday-Thursday (4pm-4: 30pm)

eastern time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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